DATA SHEET

UAA3545
Fully integrated DECT transceiver

Product specification
File under Integrated Circuits, IC17

2001 Sep 06

Philips
Semiconductors

PHILIPS

Fully integrated DECT transceiver UAA3545

FEATURES

- Economical solution for a radio in DECT cordless telephones
- Integrated low phase noise VCO with no production tuning required
- Fully integrated receiver with high sensitivity
- Dedicated DECT PLL synthesizer
- 3 dBm output preamplifier with an integrated switch
- 3-line serial interface bus
- Low current consumption from a 3.2 V supply
- Compatible with Philips Semiconductors baseband chips (PCD509xx and PCD80xxx)
- Reduced number of control signals.

APPLICATIONS

- DECT cordless telephones: 1880 to 1930 MHz.

GENERAL DESCRIPTION

The UAA3545 BiCMOS device is a low power, highly integrated circuit, for Digital Enhanced Cordless Telecommunication (DECT) applications.

It features a fully integrated receiver, from antenna filter output to the demodulated data output, a fully integrated VCO, a synthesizer to implement a phase-locked loop for DECT channel frequencies and a TX preamplifier to drive the external transmit power amplifier (CGY20xx series or UAA359x series of Philips integrated circuits).

The synthesizer's main divider is driven by the prescaler output in the range of 1880 to 1930 MHz and is programmed via a 3-wire serial bus. The reference divider ratio is programmable to 4, 8, 12 or 16. Outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter (only a passive loop filter is necessary). The charge-pump current is set to 4 mA for fast switching.

The VCO is powered from an internally regulated voltage source and includes integrated variable capacitance diodes and integrated coils. Its tuning range is guaranteed. The VCO and the synthesizer are switched-on one slot before the active slot to lock the VCO to the required channel frequency. Immediately before the active slot, the synthesizer is switched-off to allow open loop modulation of the VCO during transmission. When opening the loop, frequency pulling (due to switching-off the synthesizer) can be maintained within the DECT specification.

The device is designed to operate from a 3.2 V nominal supply. Separate power and ground pins are provided for the different sections of the circuit. Ground leads should be short-circuited externally to prevent large currents flowing across the die and causing damage. All V_{CC} supplies ($V_{CC(REG)}$, $V_{CC(SYN)}$, $V_{CC(RX)}$ and $V_{CC(TX)}$) must be at the same potential (V_{CC}).

ORDERING INFORMATION

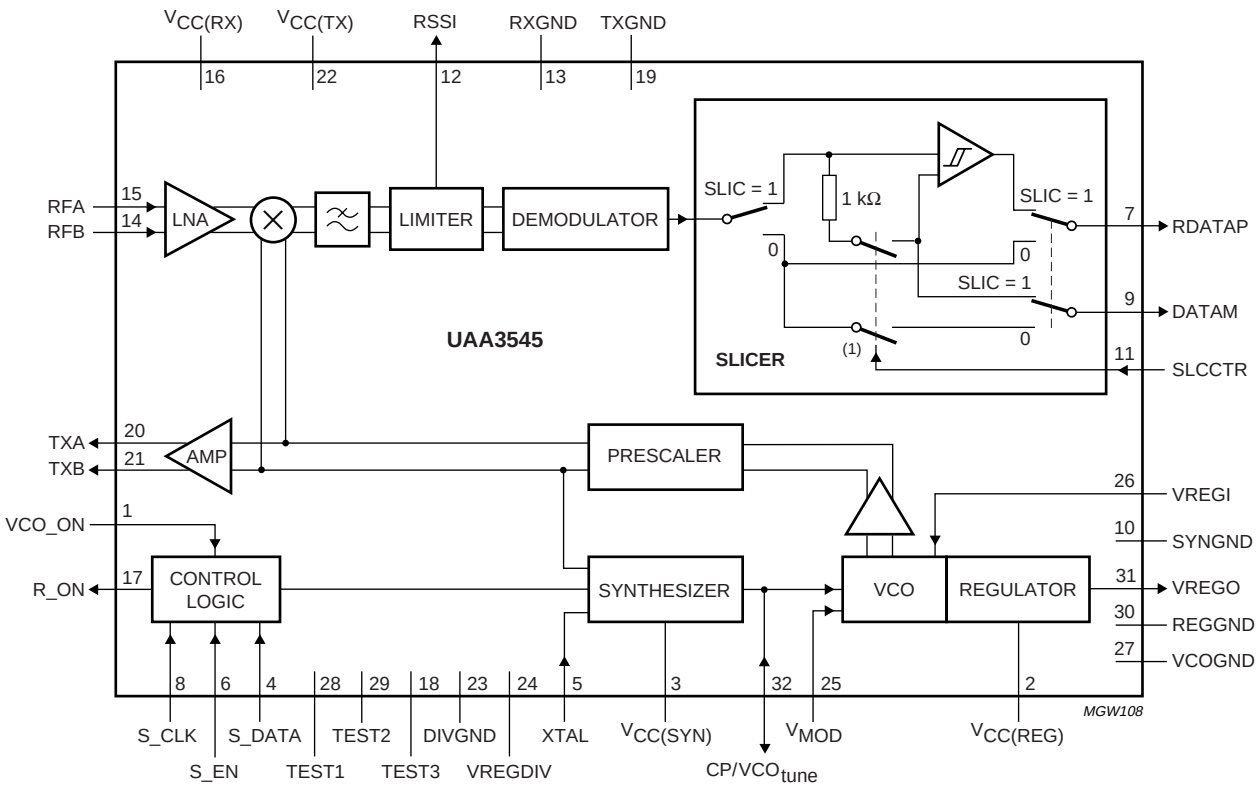
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3545HL	LQFP32	plastic low profile quad flat package; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1

QUICK REFERENCE DATA

V_{CC} = 3.2 V; T_{amb} = 25 °C; characteristics with a typical value only are not tested; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(syn)}$, $V_{CC(reg)}$, $V_{CC(RX)}$, $V_{CC(TX)}$	supply voltage	All V_{CC} supplies must be at the same potential (V_{CC})	3.0	3.2	3.6	V
$I_{CC(SYN)}$	synthesizer supply current	synthesizer ON	–	5	7	mA
$I_{CC(REG)}$	VCO, buffer and prescaler regulator supply current	VCO ON	–	14	17	mA
$I_{CC(RX)}$	receiver supply current		–	36	44	mA
$I_{CC(TX)}$	transmit preamplifier supply current		–	12	15	mA
$I_{CC(pd)}$	total supply current in Power-down mode		–	10	100	µA
$f_{o(RF)}$	RF output frequency		1880	–	1930	MHz
$f_{(i)XTAL}$	crystal reference input frequency		–	3.456, 6.912, 10.368 or 13.824	–	MHz
f_{PC}	phase comparator frequency		–	864	–	kHz
T_{amb}	ambient temperature		–10	–	+60	°C

BLOCK DIAGRAM



(1) SLCCTR ‘switches’ shown in position SLCCTR = LOW.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VCO_ON	1	VCO section power-on control; note 1
$V_{CC(REG)}$	2	regulator positive supply voltage
$V_{CC(SYN)}$	3	synthesizer positive supply voltage
S_DATA	4	3-wire bus data signal input
XTAL	5	reference frequency input; note 2
S_EN	6	3-wire bus enable signal input
RDATAP	7	demodulator output voltage
S_CLK	8	3-wire bus clock signal input
DATAM	9	switched demodulator output voltage
SYNGND	10	synthesizer ground
SLCCTR	11	DATAM switch control signal (see Fig.1)
RSSI	12	received signal strength intensity voltage output
RXGND	13	receiver ground
RFB	14	received signal input B
RFA	15	received signal input A
$V_{CC(RX)}$	16	receiver positive supply voltage
R_ON	17	receiver power-on control; note 3
TEST3	18	TEST input 3 (must be connected to GND)
TXGND	19	transmitter ground
TXA	20	transmit amplifier output A
TXB	21	transmit amplifier output B
$V_{CC(TX)}$	22	transmitter positive supply voltage
DIVGND	23	divider ground
VREGDIV	24	divider regulated supply voltage
V_{MOD}	25	VCO analog modulation voltage input
VREGI	26	VCO regulated voltage input
VCOGND	27	VCO ground
TEST1	28	TEST input 1 (must not be connected)
TEST2	29	TEST input 2 (must not be connected)
REGGND	30	regulator ground
VREGO	31	VCO section regulated voltage output
CP/VCO_{tune}	32	charge-pump output/VCO tuning input

Notes

1. Corresponds to the S_PWR of the baseband chip (see Section “Operating modes” for more details).
2. Corresponds to the REF_CLK of the baseband chip.
3. See Section “Operating modes” for more details.

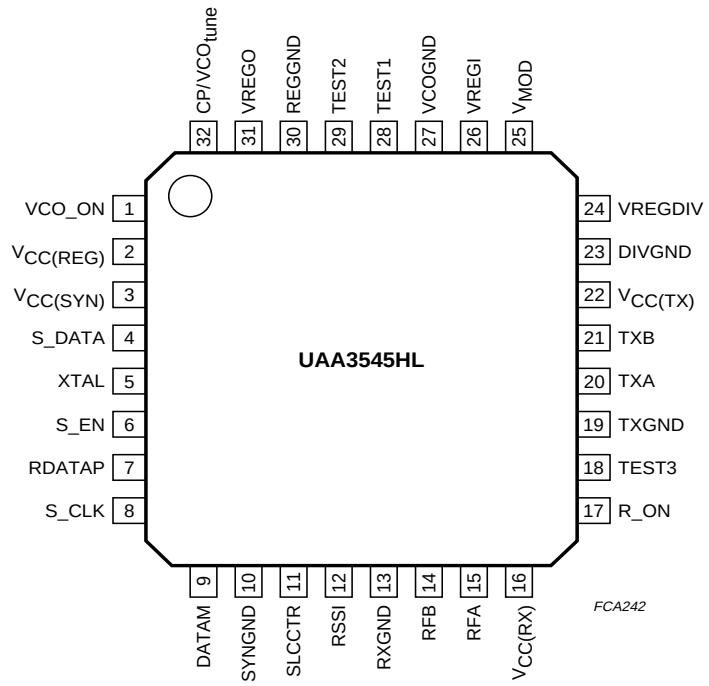


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Transmit chain

VCO AND PRESCALER

The fully integrated VCO operates at a multiple of the DECT frequency. It is supplied by an on-chip voltage regulator to minimize frequency disturbances due to supply voltage variations. The VCO signal is fed into a prescaler. A large difference between transmitted and VCO frequencies reduces transmitter-oscillator coupling problems.

The output of the prescaler drives the synthesizer main divider. The divider output can also be switched to either the TX preamplifier or the RX LO output buffer. The high isolation obtained from the prescaler ensures very small frequency changes when turning-on the TX preamplifier or the RX section. In TX mode, the oscillator can be modulated directly with GFSK-filtered data at pin V_{MOD}.

TX PREAMPLIFIER

The TX preamplifier amplifies the RF signal to a level of 3 dBm (typical) which is suitable for use with Philips Semiconductors DECT power amplifiers.

Synthesizer

MAIN DIVIDER

The main divider is clocked by the RF signal from the prescaler at frequencies from 1880 to 1930 MHz. Any main divider ratio from 2176 to 2303 inclusive can be programmed.

REFERENCE DIVIDER

The reference divider is clocked by the signal at pin XTAL. The circuit operates with levels from 1.2 to 1.8 V (p-p) at a frequency of 3.456 MHz. By programming the ‘REFD’ bits of the serial input register (see Table 1) the reference frequency can be set for 6.912, 10.368 or 13.864 MHz.

PHASE COMPARATOR

The phase comparator is driven by the output of the main and reference dividers. It produces current pulses at pin CP/VCO_{tune}, the pulse duration being the difference in arrival time of current pulse edges from the two dividers. If the main divider edge arrives first, pin CP sinks current. If the reference divider edge arrives first, pin CP sources current. The DC value of the charge-pump current is defined by an internal resistor. Additional circuitry is included to ensure the gain of the phase detector remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The three lines are data (S_DATA), serial clock (S_CLK) and serial bus enable (S_EN). Data sent to the device are loaded in bursts framed by S_EN. Programming clock edges and their appropriate data bits are ignored until S_EN goes active (LOW). The programmed information is read directly by the main divider when S_EN returns to HIGH. S_DATA and S_EN change value on the falling edge of S_CLK.

During synthesizer operation, S_EN should be held HIGH. Only the last 24 bits clocked into the device are retained within the serial register. Additional leading bits are ignored and no check is made on the number of clock pulses. The data format is shown in Table 1. The first bit entered is b23, the last bit is b0. For the main divider ratio, the first bit (b5) is the Most Significant Bit (MSB).

The serial bus enable (S_EN) must be LOW to capture new programming data and must be HIGH to switch on the synthesizer.

Receiver

The receiver is a fully integrated RF + IF strip and demodulator for DECT. It provides all the required channel filtering over the DECT band and generates analog RSSI and a switched output for Philips Semiconductors baseband chip. Very few off-chip components are required and all of these can be placed without trimming. The chip is designed to operate with a power supply voltage that can fall to 3.0 V. The input is the RF antenna signal derived from the band filter or the antenna switch. The outputs are the RSSI voltage, representing the instantaneous signal strength and two HIGH-level demodulator output signals RDATAP and DATAM, the latter being switched by SLCCTR to generate the external slicer threshold. During the blind slot, while the PLL is settling, an internal voltage source is activated to precharge the external capacitor (connected to pin DATAM) to a voltage close to the required slicer threshold.

Operating modes

The operating modes available are:

- Normal mode (see Fig.3)
- Reduced signal mode (see Fig.4)
- Advanced signal mode (see Fig.5).

Selection of an operating mode is achieved via the serial interface register (see Table 3).

NORMAL MODE (MODE 1)

In the normal mode, the synthesizer is ON when S_EN = HIGH and VCO_ON = HIGH, and OFF when S_EN = LOW. When turned ON, the dividers and phase detector are synchronized to avoid a random initial phase error. When turned OFF, the phase detector is synchronized with the dividers to avoid interrupting a charge-pump pulse. This feature requires a signal to be present for a few microseconds on the XTAL pin after S_EN goes LOW.

The VCO is ON when the input signal VCO_ON is HIGH. The polarity of VCO_ON is chosen for compatibility with output S_PWR of the baseband chip. When the VCO is turned ON, it takes 50 μs (typical) to reach its steady state.

The TX preamplifier is ON when bit ‘TRX’ is programmed to ‘0’ and VCO_ON is HIGH. When the TX preamplifier is turned ON, it takes typically 10 μs to be ready. The receiver is turned ON when R_ON = HIGH and VCO_ON = HIGH.

REDUCED SIGNAL MODE (MODE 2)

In the reduced signal mode, the parallel control signals are replaced by serial bus programming. To select this mode, the bit ‘NEW’ of the internal register must be set to ‘1’ and the bit ‘SPWR’ must be reset to ‘0’, timing is then controlled by the S_EN signal.

After the register programming, the S_EN rising edge programs the PLL, closes the loop, powers-on the VCO and, if the ‘TRX’ bit = 0, turns ON the TX preamplifier. On the falling edge of the first S_EN pulse, the loop is opened (unless the bit ‘PLL’ is set to 1) and the receiver switches ON if the ‘TRX’ bit = 1. A second pulse on S_EN is required at the end of the wanted slot to power-down the application.

The R_ON pin becomes an output in this mode, drives the RX PIN diode and corresponds to the internal power-on signal of the receiver.

ADVANCED SIGNAL MODE (MODE 3)

In the advanced signal mode, the parallel control signals are partly replaced by serial bus programming. To select this mode, the bit ‘NEW’ and the bit ‘SPWR’ of the internal register must be set to ‘1’. The S_EN signal will then control the UAA3545 timing (except for timing of a general power-down as this is controlled by the VCO_ON input).

The VCO_ON signal should rise at the beginning of the previous slot. After the serial bus has been programmed, the S_EN rising edge programs the PLL, closes the loop and, if the ‘TRX’ bit = 0, turns ON the TX preamplifier. On the falling edge of the first S_EN pulse, the loop is opened (unless the ‘PLL’ bit is set to 1) and the RX section switches ON if bit ‘TRX’ = 1. At the end of the wanted slot, the VCO_ON goes LOW to power-down the whole IC. In fact, the second pulse of the S_EN signal in mode 2 is now replaced by the signal VCO_ON.

The R_ON pin becomes an output in this mode, drives the RX PIN diode and corresponds to the internal power-on signal of the receiver.

Programming

Table 1 Serial interface register

REGISTER BIT ALLOCATION								
first in								**last in**
b23 to b20	b19	b18, b17	b16 to b10	b9	b8	b7	b6	b5 to b0[1]
TEST[2]	SLIC[3]	REFD[4]	TEST[2]	SPWR[5]	PLL[6]	NEW[5]	TRX	MAIN DIVIDER[7]

Notes

1. Bit b5 is the MSB of the main divider coefficient; this comprises bits b5, b4, b3, b2, b1, b0 and b6 (TRX).
2. Test bits b23, b22, b21, b20, b16, b15, b14, b13, b12, b11, b10 must always be programmed to 0.
3. Bit ‘SLIC’ = 1 forces the internal slicer on. In this mode, pin DATAM is connected to an external capacitor. Together with an internal 1 kΩ resistor, it defines the low pass time constant for the slicer threshold voltage. When the bit ‘SLIC’ = 0, the pin RDATAP is connected directly to the demodulator output and delivers an analog signal. Pin DATAM also reflects the demodulator voltage without the internal 1 kΩ resistor when the SLCCTR pin is HIGH.
4. REFD sets the reference divider ratio to 4, 8, 12 or 16 (corresponding respectively to a reference input frequency of 3.456, 6.912, 10.368 or 13.824 MHz) (see Table 4).
5. Bits ‘NEW’, and ‘SPWR’ select the operating mode (see Table 3).
6. Bit ‘PLL’ = 1 forces the PLL to remain on when the VCO is on.
7. The main divider ratio is equal to 2176 + the programmed value (see Table 2).

Table 2 Main divider programming

BIT							MAIN DIVIDER RATIO	SYNTHESIZED FREQUENCY (MHz)
b5	**b4**	**b3**	**b2**	**b1**	**b0**	**b6 (TRX)**		
Binary equivalent of n							2176 + n	0.864 × (2176 + n)
0	0	0	0	0	0	0	2176	1880.064
0	1	0	1	1	1	1	2223	1920.672

Table 3 Operating mode selection

BIT		OPERATING MODE
b9 (SPWR)	**b7 (NEW)**	
0	0	normal mode (mode 1)
0	1	reduced signal mode (mode 2)
1	0	do not use
1	1	advanced signal mode (mode 3)

Table 4 Reference divider ratio programming

BIT		REFERENCE DIVIDER RATIO	REFERENCE INPUT FREQUENCY
b18	**b17**		
0	0	4	3.456 MHz
0	1	16	13.824 MHz
1	0	8	6.912 MHz
1	1	12	10.368 MHz

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(syn)}$, $V_{CC(reg)}$, $V_{CC(RX)}$, $V_{CC(TX)}$	supply voltage	All V_{CC} supplies must be at the same potential (V_{CC})	−0.3	+3.6	V
V_n	voltage on any pin		−0.3	V_{CC}	V
$P_{i(RFA)(max)}$, $P_{i(RFB)(max)}$	maximum input power at pins RFA and RFB		–	15	dBm
ΔGND	difference in ground supply voltage applied between all ground pins	note 1	–	0.01	V
P_{tot}	total power dissipation		–	300	mW
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature		−10	+60	°C
T_j	junction temperature		–	150	°C

Note

1. Ground pins must be short-circuited externally (this is in addition to being short-circuited internally.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

All pins are compatible with *“EIA/JESD22-A114-A Class1 (October 1997)”*.

LATCH-UP

Pins S_DATA, TXA and TXB are susceptible to latch-up if a negative current greater than 20 mA is drawn from the respective pin (occurs when the pin voltage is negative with respect to GND).

To avoid latch-up, pins TXA and TXB pins must be connected to V_{CC} through coils, and the S_DATA control signal input from the baseband IC must be kept positive with respect to GND.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

CHARACTERISTICS

V_{CC} = 3.2 V; T_{amb} = 25 °C; f_{dev} = 288 kHz; $f_{(i)XTAL}$ = 13.824 MHz; characteristics with a typical value only are not tested; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{CC(syn)}$, $V_{CC(reg)}$, $V_{CC(RX)}$, $V_{CC(TX)}$	supply voltage	All V_{CC} supplies must be at the same potential (V_{CC})	3.0	3.2	3.6	V
$I_{CC(SYN)}$	synthesizer supply current	S_EN = HIGH	–	5	7	mA
$I_{CC(REG)}$	VCO, buffer and prescaler regulator supply current	VCO ON	–	14	17	mA
$I_{CC(RX)}$	receiver supply current	RX mode	–	36	44	mA
$I_{CC(TX)}$	transmit preamplifier supply current	TX mode	–	12	15	mA
$I_{CC(pd)}$	total supply current in Power-down mode		–	10	100	μA
Synthesizer						
MAIN DIVIDER						
$f_{o(RF)}$	RF output frequency		1880	–	1930	MHz
R_m	main divider ratio		2176	–	2234	
REFERENCE DIVIDER						
$f_{(i)XTAL}$	crystal reference input frequency	programmed values; see Table 4	–	3.456, 6.912, 10.368 or 13.824	–	MHz
$V_{(i)XTAL(p-p)}$	crystal reference input voltage (peak-to-peak value)	square wave input; all $f_{(i)XTAL}$ values	1.2	–	1.8	V
R_{RD}	reference divider ratio	programmed values; see Table 4	–	4, 8, 12 or 16	–	
$R_{i(XTAL)}$	input resistance (real part of the parallel input impedance)	$f_{(i)XTAL}$ = 3.456 MHz	–	17	–	kΩ
$C_{i(XTAL)}$	input capacitance (imaginary part of the parallel input impedance)	$f_{(i)XTAL}$ = 3.456 MHz	–	1.5	–	pF
PHASE COMPARATOR						
f_{PC}	phase comparator frequency		–	864	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE-PUMP OUTPUT						
$I_{o(CP)}$	charge-pump output current	$V_{CP} = ½V_{CC}$	–	3.5	–	mA
VCO						
f_{VCO}	oscillator frequency	defined at transmit output, T_{amb} = –10 to +60 °C; note 1	1880	–	1930	MHz
$V_{CP/VCOtune}$	charge pump input voltage and VCO tuning output voltage		0.3	–	V_{CC} – 0.3	V
G_{VCO}	VCO tuning input gain (mean value)	defined at transmit output; note 2	–	70	–	MHz/V
G_{MOD}	VCO modulation input gain	defined at transmit output; note 3	–	2.4	–	MHz/V
Transmit preamplifier						
$P_{o(TXA)}$, $P_{o(TXB)}$	transmit output power	T_{amb} = –10 to +60 °C; f_{VCO} = 1880 to 1930 MHz; note 1	0	3	–	dBm
$R_{o(TXA)}$, $R_{o(TXB)}$	transmit output resistance (real part of the parallel output impedance)	balanced; expressed at high signal level	–	200	–	Ω
$C_{o(TXA)}$, $C_{o(TXB)}$	transmit output capacitance (imaginary part of the parallel output impedance)	balanced; expressed at high signal level	–	0.3	–	pF
$f_{VCO(feedthru)}$	VCO frequency feedthrough at transmit output	referred to $P_{o(TXA)}$, $P_{o(TXB)}$; f_{VCO} = 1900 MHz; note 1	–	–20	–15	dBc
CNR_{25}	carrier-to-noise ratio at transmit output	carrier offset in closed loop; Δf = 25 kHz	–	–65	–56	dBc/Hz
CNR_{4686}	carrier-to-noise ratio at transmit output	carrier offset; Δf = 4686 kHz	–	–135	–129	dBc/Hz
$\Delta f_{o(push)}$	frequency shift due to supply voltage drop	measured dynamically; V_{CC} drop = 100 mV; $V_{CP/VCOtune}$ = 1.2 V; V_{MOD} = 0; TX load = 50 Ω; note 1	–	+10	±20	kHz
$\Delta f_{o(pull)}$	frequency shift due to disabling the synthesizer	frequency pulling measured 20 μs after synthesizer disabled; $V_{CP/VCOtune}$ set by the PLL on f_{VCO} = 1880.064 MHz; V_{MOD} = 0; TX load = 50 Ω; note 1	–	+5	±10	kHz
$\Delta f_{o(drift)}$	transmit output frequency drift during a slot	notes 1 and 4	–	–6	±12	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver section						
$V_{RSSI(max)}$	maximum RSSI output voltage	under high RX input signal level	–	1.9	–	V
V_{RSSI}	RSSI output voltage	monotonicity over range –96 to –36 dBm				
		$P_{i(RFA/B)}$ = –33 dBm	–	1.7	2.0	V
		$P_{i(RFA/B)}$ = –36 dBm	–	1.64	–	V
		$P_{i(RFA/B)}$ = –96 dBm	–	0.3	–	V
t_{on}	wake-up time from the power-on signal to correct RSSI output		–	25	40	µs
s_B	input sensitivity	BER ≤ 10^{-3}; note 1	–	–96	–93	dBm
		BER ≤ 10^{-5}; note 1	–	–92	–76	dBm
IM	intermodulation rejection	BER < 10^{-3}; wanted signal at –83 dBm; level of interference in channels n + 2 and n + 4; note 1	33	42	–	dBc
R_{co}	co-channel rejection	BER < 10^{-3}; wanted channel at –76 dBm; note 1	–10	–7.5	–	dBc
$R_{i(n-1)}$	adjacent channel rejection	BER < 10^{-3}; wanted channel at –76 dBm; adjacent level referred to wanted channel level; note 1	14	20	–	dBc
$R_{i(n-2)}$	bi-adjacent channel rejection	BER < 10^{-3}; wanted channel at –76 dBm; bi-adjacent level referred to wanted channel level; note 1	35	42	–	dBc
$R_{i(n-\geq 3)}$	rejection with ≥3 channels separation	BER < 10^{-3}; wanted channel at –76 dBm; n ≥ 3 adjacent level referred to wanted channel level; note 1	40	45	–	dBc
RBI	rejection of a blocking signal	BER < 10^{-3}; wanted signal at –83 dBm at channel 5:				
		$\lvert f - f_c \rvert$ > 6 MHz; note 2	38	55	–	dBc
		(f_{RFmax} + 5 MHz) < f < 2 GHz; 1780 MHz < f < (f_{RFmin} – 5 MHz); note 1	48	58	–	dBc
		2 GHz < f < 4.32 GHz; notes 1 and 5	38	60	–	dBc
$R_{o(RF)}$	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	100	–	Ω
$C_{o(RF)}$	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	0.8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{i(RF)(max)}$	maximum RF input frequency		–	–	1930	MHz
$f_{i(RF)(min)}$	minimum RF input frequency		1880	–	–	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{DEM}	demodulator gain	mean value of f_{dev} = ±288 kHz	–	1.6	–	V/MHz
V_{DEM}	DC level at demodulator outputs RDATAP and DATAM	$f_{LO} = f_{RF}$ + 864 kHz	–	1.3	–	V
Interface logic input and output pins S_DATA, S_CLK, S_EN, R_ON, VCO_ON, SLCCTR and RDATAP						
V_{IH}	HIGH-level input voltage	note 6	1.4	–	V_{CC}	V
V_{IL}	LOW-level input voltage)		–0.3	–	+0.4	V
I_{bias}	input bias current	HIGH or LOW input levels	–5	–	+5	µA
$V_{OH(RDATAP)}$	HIGH-level output voltage (pin RDATAP)	bit ‘SLIC’ = 1; I_{OH} = 500 µA	V_{CC} – 0.4	V_{CC}	–	V
$V_{OL(RDATAP)}$	LOW-level output voltage (pin RDATAP)	bit ‘SLIC’ = 1; I_{OL} = –500 µA	–	0	0.4	V
$I_{O(RON)}$	output drive current (pin R_ON)	mode 2 or 3; V_{RON} = HIGH level; $V_{CC} - V_{RON}$ = 0.5 V	2.5	5	–	mA
$Z_{O(RON)}$	output impedance (pin R_ON)	mode 2 or 3; V_{RON} = LOW level	–	6	–	kΩ
$f_{SCLK(max)}$	maximum frequency (pin S_CLK)		–	10	–	MHz
$t_{SEN(min)}$	minimum pulse duration (pin S_EN)		–	1	–	µs

Notes

1. Measured and guaranteed only on the Philips evaluation board, including Printed-Circuit Board (PCB) and balun filter with internal slicer.
2. Mean of the values of transmit frequency at $V_{CP/VCOtune}$ = 0.3 and 2.7 V.
3. Measured with $V_{CP/VCOtune}$ = 1.5 V, mean of the values of transmit frequency at V_{MOD} = 0 and 0.5 V.
4. Frequency difference measured during 420 µs with V_{MOD} = 0 (no modulation applied), at least 20 µs after disabling the synthesizer.
5. Except for three occurrences, as defined in the DECT specification.
6. V_{IH} should never exceed 3.6 V.

MODE 1 TIMING

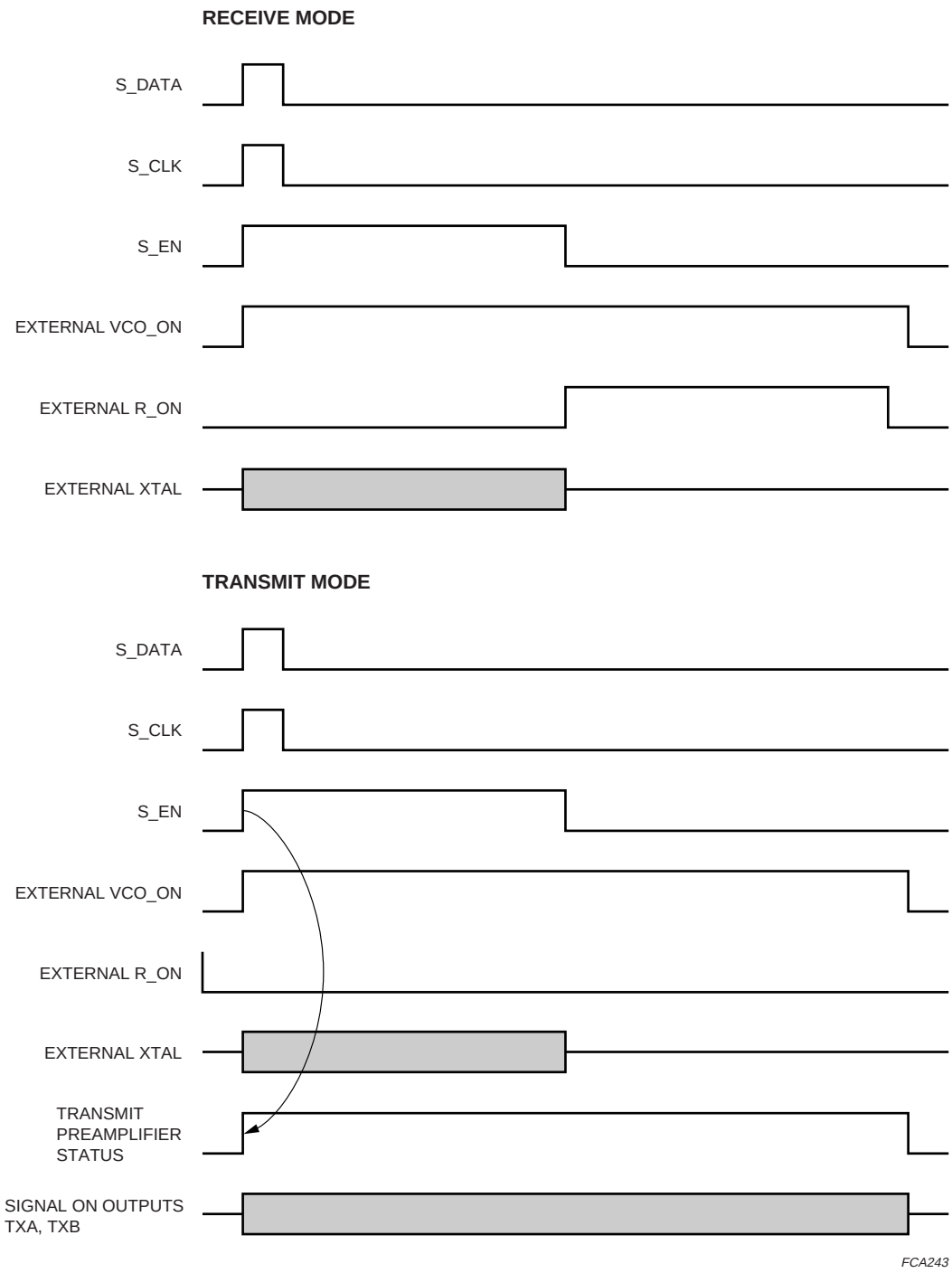


Fig.3 Normal mode timing diagram.

MODE 2 TIMING

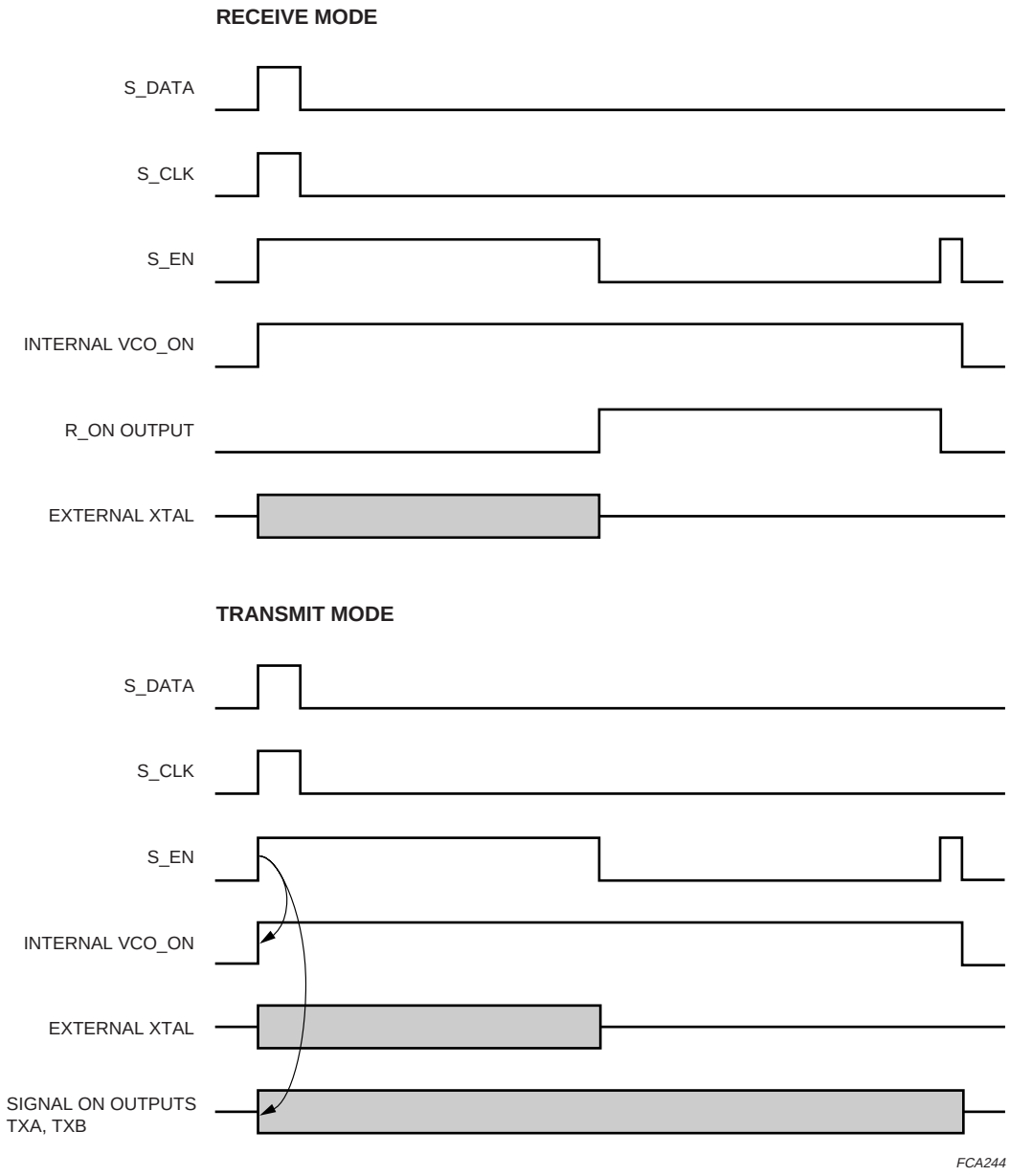


Fig.4 Reduced signal mode timing diagram.

MODE 3 TIMING

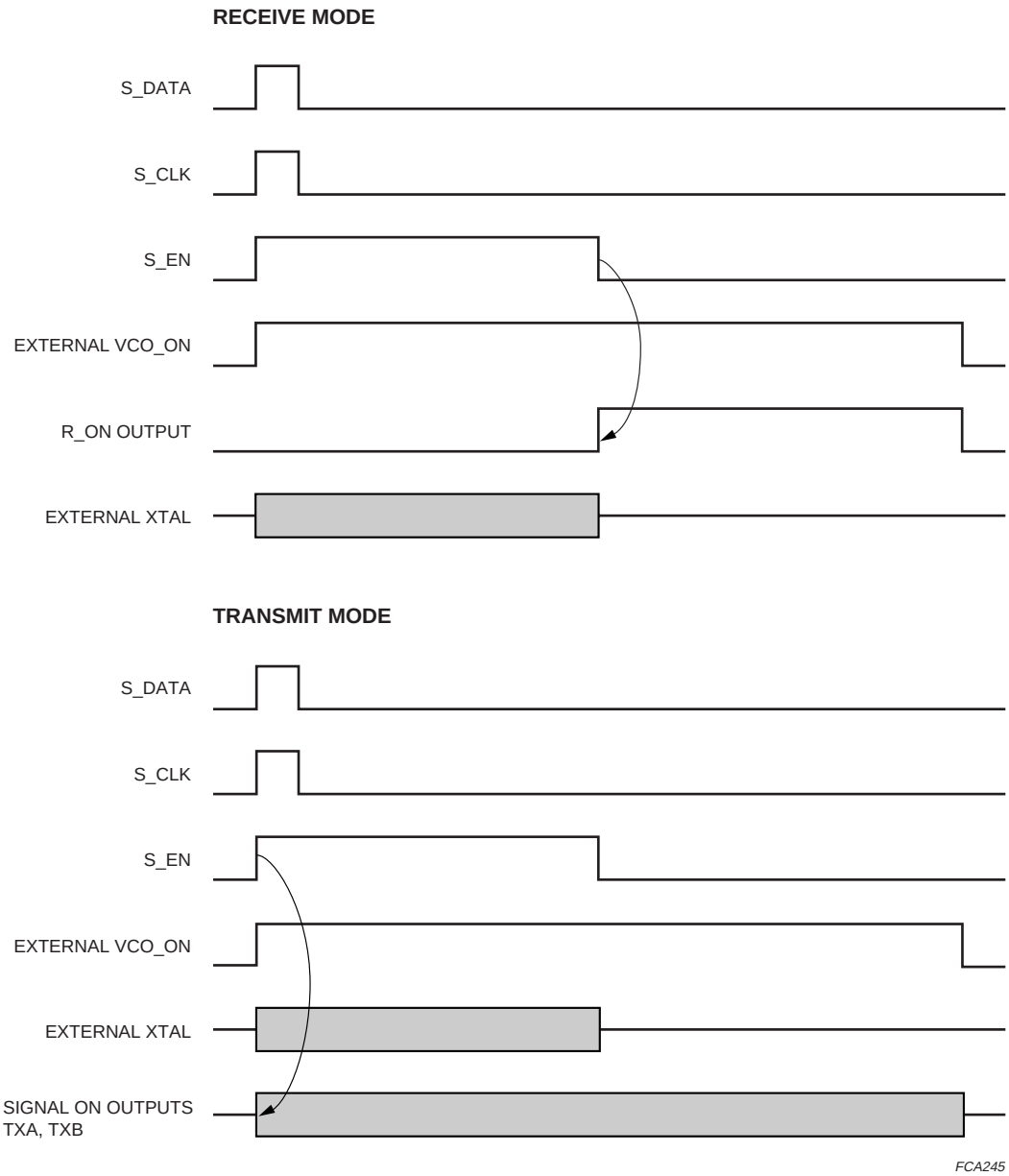


Fig.5 Advanced signal mode timing diagram.

APPLICATION INFORMATION

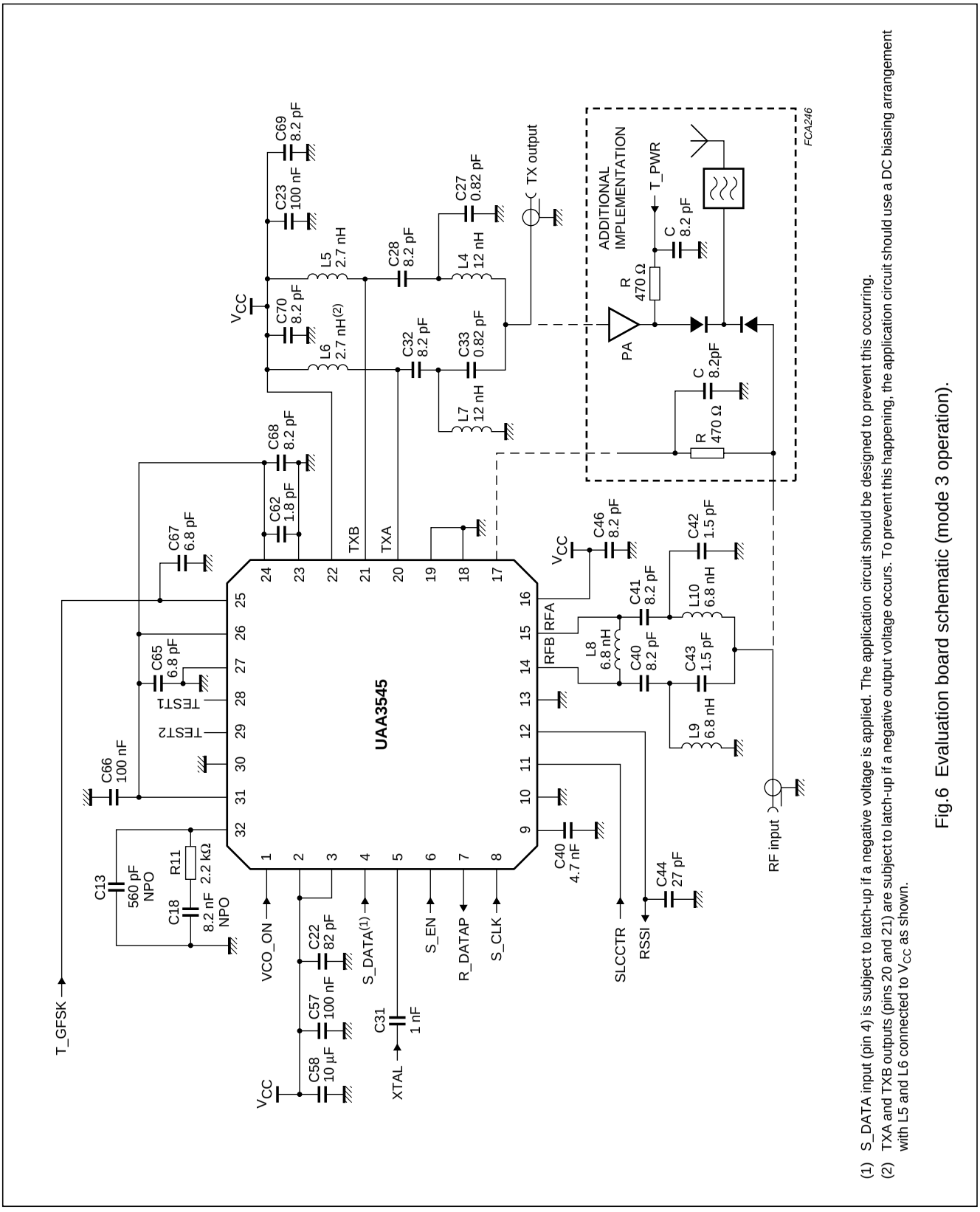
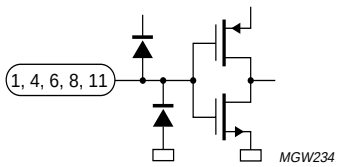
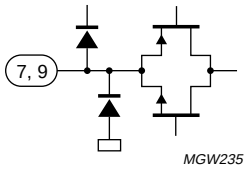
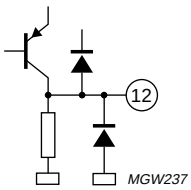
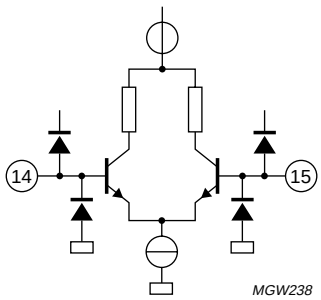
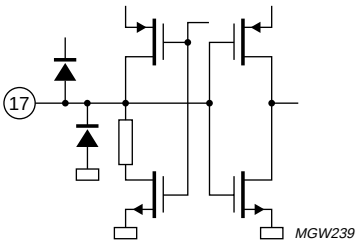


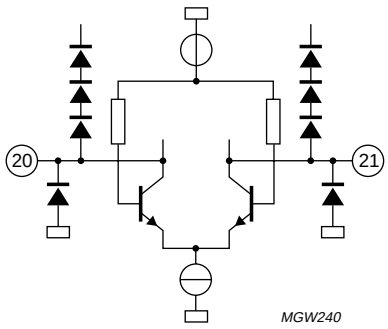
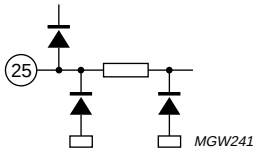
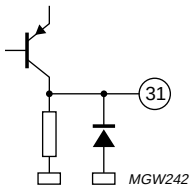
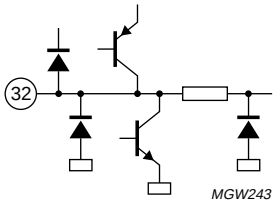
Fig.6 Evaluation board schematic (mode 3 operation).

(1) S_DATA input (pin 4) is subject to latch-up if a negative voltage is applied. The application circuit should be designed to prevent this occurring.

(2) TXA and TXB outputs (pins 20 and 21) are subject to latch-up if a negative output voltage occurs. To prevent this happening, the application circuit should use a DC biasing arrangement with L5 and L6 connected to V_{CC} as shown.

Internal pin configuration

PIN	SYMBOL	INTERNAL CIRCUIT
1	VCO_ON	
4	S_DATA	
6	S_EN	
8	S_CLK	
11	SLCCTR	
7	RDATAP	
9	DATAM	
12	RSSI	
14	RFB	
15	RFA	
17	R_ON	

PIN	SYMBOL	INTERNAL CIRCUIT
20	TXA	
21	TXB	
25	V_{MOD}	
31	VREGO	
32	CP/VCO_{tune}	

RECEIVED SIGNAL STRENGTH INTENSITY

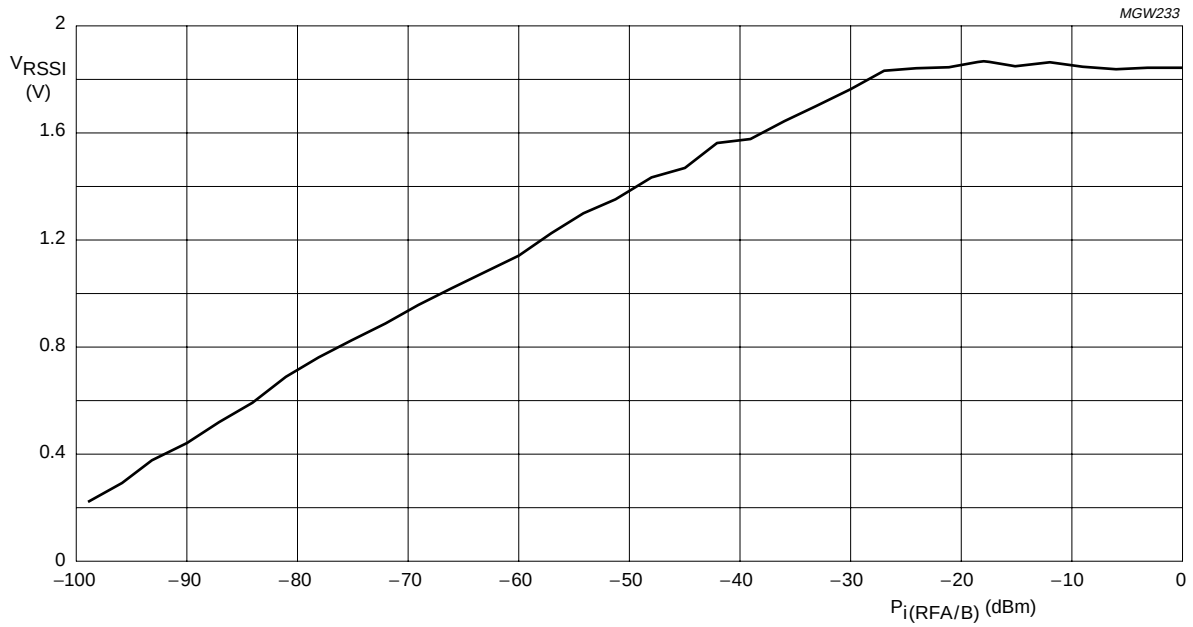
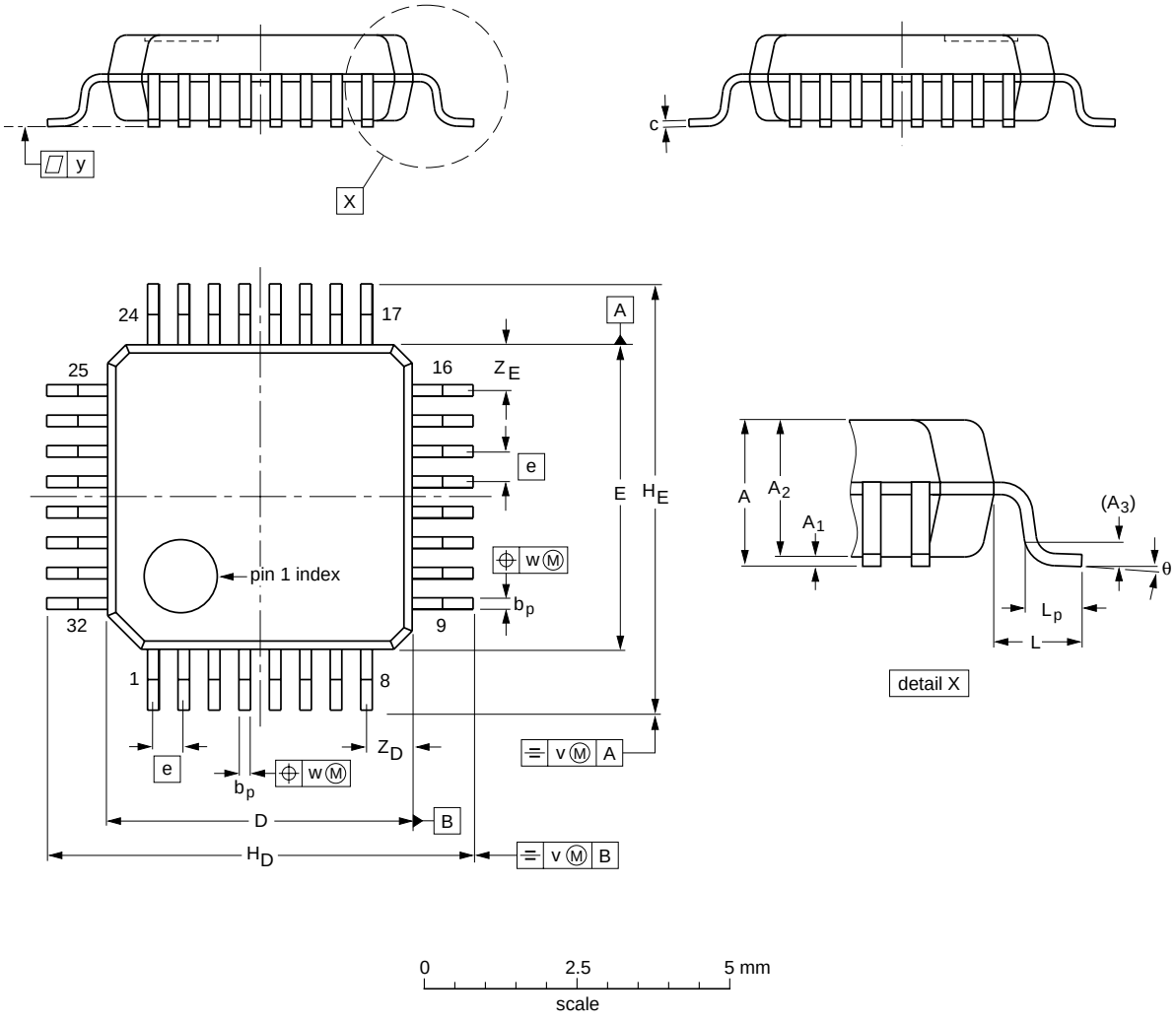


Fig.7 RSSI output as a function of input power at pins RFA and RFB.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1	136E01	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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